WHAT IS CLAIMED IS:

1. A multiprocessor system having a plurality of nodes, each node including at least one CPU, at least one Translation Lookaside Buffer (TLB), each associated with a respective Central Processing Unit (CPU), and a local main memory forming a part of a main memory space of the multiprocessor system, and an inter-node network, each of the nodes further comprising:

a map table having entries corresponding to respective physical pages of said local main memory and storing correspondence between each physical page number of said physical pages and a virtual page number actually mapped to each physical page number;

network transaction generating means for generating, when a result of an address translation using a TLB indicates that a memory access request from a CPU is to be directed to a local maim memory of another node, a network transaction corresponding to said memory access request which includes a physical address to be accessed obtained from said result of the address translation using the TLB and a virtual page number designated in said memory access request from the CPU;

transaction receiving means for receiving network transactions transferred from other nodes;

checking means for checking for coincidence between a first virtual page number which is included in a received network transaction and a second virtual page number obtained through reference to said map table using a physical address included in the received memory access transaction; and

main memory access means for executing an access to said local main

memory corresponding to said received network transaction when said first and second virtual page numbers are coincident.

2. A Multiprocessor system according to claim 1, wherein said map table stores a plurality of virtual pages mapped to a physical page.

3. A Multiprocessor system according to claim 1, wherein said map table further stores information indicating whether the mapping between a virtual page and a physical page is valid or not.

4. A Multiprocessor system according to claim 1, wherein said map table is mapped to a part of a memory space of said multiprocessor system.

5. A Multiprocessor system according to claim 1, wherein each node further includes means for selecting physical page numbers in said map table in which a mapped virtual page is stored, among all physical pages of said main memory.

6. A multiprocessor system having a plurality of nodes, each node including at least one Central Processing Unit (CPU) at least one Translation Lookaside Buffer (TLB), each associated with a respective CPU, and a local main memory forming a part of a main memory space of the multiprocessor system, and an inter-node network, each of the nodes further comprising:

a map table having entries corresponding to respective physical pages of

said local main memory and storing correspondence between each physical page number of said physical pages and a virtual page number actually mapped to said each physical page number;

network transaction generating means for generating, when a result of an address translation using a TLB indicates that a memory access request from a CPU is to be directed to a local main memory of another node, a network transaction corresponding to said memory access request which includes a physical address to be accessed obtained from said result of the address translation using the TLB and a virtual page number designated in said memory access request from the CPU;

transaction receiving means for receiving network transactions transferred from other nodes;

checking means for checking for coincidence between a first virtual page number which is included in a received network transaction and a second virtual page number obtained through reference to said map table using a physical address included in the received memory access transaction;

main memory access means for executing an access to said local main memory corresponding to said received network transaction when said first and second virtual page numbers are coincident; and

error message generating means for informing a source of said received network transaction of an error when said first and second virtual pages are not coincident.

7. A Multiprocessor system according to claim 6, wherein said map table stores a plurality of virtual pages mapped to a physical page.

8. A Multiprocessor system according to claim 6, wherein said map table further stores information indicating whether the mapping between a virtual page and a physical page is valid or not.

9. (Amended) A Multiprocessor system according to claim 6, wherein said map table is mapped to a part of a memory space of said multiprocessor system.

10. A Multiprocessor system according to claim 6, wherein each node further includes means for selecting physical page numbers in said map table in which a mapped virtual page is stored, among all physical pages of said main memory.